

Serial No. 09/605,293
Atty. Docket No. MIO 0037.VA

D1
chemical vapor deposition (PECVD), metalorganic chemical vapor deposition (MOCVD), and sputtering. The layer 18 of polycrystalline silicon 20 is formed on the layer 14 of silicon dioxide 16 by any deposition process currently used in the art to form a layer of polycrystalline silicon on a layer of silicon dioxide. Useful deposition methods include, but are not limited to, CVD, LPCVD, PECVD, MOCVD and sputtering.

At page 9, lines 17-21 should read:

D2
After the hydrogen ions have been implanted into the layer 14 of silicon dioxide 16, the layer 18 of polycrystalline silicon 20 is formed on the layer 14. The layer 18 of polycrystalline silicon 20 is formed on the layer 14 by any deposition method currently in use in the art. Useful deposition methods include, but are not limited to, CVD, LPCVD, PECVD, MOCVD and sputtering.

At page 10, lines 21-28 should read:

D3
Fig. 2 presents a cross sectional view of a field effect transistor 50 formed by the method of the present invention. The field effect transistor 50 is formed on semiconductor substrate 52. The field effect transistor 50 includes a gate oxide 54, a source 56 and a drain 58. The gate oxide 54, the source 56 and the drain 58 are formed in the substrate 52. A layer 64 of polysilicon 66 is formed on the gate oxide 54 to form a gate electrode 70. A pair of spacers 68 are formed on the sides of the layer 64 of polysilicon 66. A layer 72 of a field oxide 74 is also formed on the substrate 52.

At page 13, lines 2-9 should read:

D4
A thin film transistor 200 is shown in cross section in Fig. 5. The thin film transistor 200 includes an insulating substrate 202. A layer 204 of a semiconducting material 206 is formed on the surface of the substrate 202. A source region 208 and a drain region 210 are formed on the layer 204 of semiconducting material 206. A layer 212 of a dielectric material 214 is formed on the layer 204 of semiconducting material 206 and covers the source 208 and the drain 210. A layer 216 of a conducting material 218 is formed on the layer 212 of dielectric material 214 to form a gate electrode 220.